REMARKS

Applicant thanks the Examiner for the careful consideration given to the subject application in the Office Action dated December 17, 2004 and for the courtesy extended during a telephone interview on March 9, 2005.

By this amendment, claims 1-21 and 23-29 are currently pending in the subject application. Claims 27-29 are allowed. Claims 1-3, 6, 7, 11, 12, 15, 20, 21 and 23 presently stand rejected.

Claims 4-5, 8-10, 13-14, 16-19, 22 and 24-26 have been indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. INTERVIEW SUMMARY

Applicant, through its undersigned representative, confirms the substance of the interview on March 9, 2005 with Examiner Lam T. Mai in which the Examiner indicated that claims 24 through 26 were indicated as being allowable not as allowed as shown on the office action summary. Applicant was provided with a corrected Office Action via facsimile on March 10, 2005. This response, therefore, responds to the information contained in the reissued action.

II. Rejection of Claims 1, 15 and 23 Under 35 U.S.C. §102(e)

Claims 1, 15, and 23 stand rejected under 35 U.S.C. Section 102(e) as being anticipated by U.S. Patent No. 5,870,047 to Piesinger ("Piesinger"). Applicant traverses this rejection for at least the following reasons.

In contrast to claim 1, it is respectfully submitted that Piesinger fails to teach or even suggest an aggregator that provides an aggregated output stream signal at a desired output sample rate, which is different from an input sample rate, as recited in claim 1. In particular, at column 9, lines 17 through 27, Piesinger discloses four in-phase signals 38' and four quadrature phase signals 38", each set of four being combined by operating respective DACs 22' and 22''. In particular, each of the intermediate analog signals 38' and 38'' for the in-phase and quadrature-phase channel outputs are delayed by a delay output time, indicated as φ, corresponding to ¼ of a symbol period. Since there are four intermediate analog signals, each delayed by ¼ symbol period, the resulting symbol period for the in-phase and quadrature-phase channel signals, which are combined by the operational amplifiers 46, would be at the same rate. Consequently, the resulting outputs are provided at signals 26' and 26'' as analog signals. Since Piesinger fails to teach that an aggregator such that the desired output sample rate is different from an input sample rate, as recited in claim 1, Piesinger does not anticipate claim 1.

Claim 15 has been amended to incorporate the subject matter of claim 22, which has been indicated as being allowable. Accordingly, allowance of amended claim 15 and claims that depend from claim 15 is respectfully requested.

With respect to claim 23, it is respectfully submitted that Piesinger fails to teach or suggest the means for storing look-up table data representing Delta-Sigma modulated outputs indexed according to corresponding input signals each having a predetermined number of bits, as recited in claim 23. The office action fails to specify that Piesinger teaches the means for storing look-up table data as recited in claim 23, which, Applicant submits, is because no such teaching exists in Piesinger. Since the office action has failed to present a prima facie case of unpatentability regarding claim 23, claim 23 should be allowed. Further, the look-up table memory (70) taught by Piesinger is designed to simulate the waiting of pulse shaping network (32), the differencing of differencing networks (34) and the summing of summing circuits (36). See column 9, lines 1 – 4 of Piesinger, see also column 8, lines 9 – 60. Since Piesinger fails to teach any structure for storing look-up table data representing Delta-Sigma modulated outputs

indexed according to corresponding input signals, reconsideration and allowance of claim 23 are respectfully requested.

For the reasons described above, claims 1, 15 and 23 should be patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

III. Rejection of Claims 1-3, 6-7 and 11-12 Under 35 U.S.C. §102(e)

Claims 1 – 3, 6, 7, 11 and 12 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,489,908 ("Panasik"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Similar to the rejection of Piesinger, Panasik fails to teach or suggest that the output signal in Panasik is provided at a desired output sample rate, which is different from the input sample rate as recited in claim 1. With respect to claim 3, the office action contends that Panasik teaches the memory system operating rate that is less than the desired output sample rate referencing column 6, lines 9 – 21 of Panasik. However, the reference section of Panasik relates to the delay between the digital-to-analog converters of T/n, where T is the Nyquist period. Accordingly, reconsideration and allowance of claim 3 are respectfully requested.

Claims 2, 6 and 7 are allowable over Panasik for at least the reasons stated above with respect to claim 1.

With regard to claim 11, Panasik discloses that a plurality of digital-to-analog converters 120, 122, 124, 126 are utilized in parallel and that the signals from each of the plurality of DACs is obtained by clocking each of the DACs with the delayed multi phase clock signal. In contrast to the contention in the office action, Panasik fails to teach a digital-to-analog converter that converts the aggregated output stream signal to a corresponding analog signal having a center frequency functionally regulated to the desired output sample rate. Instead, as mentioned above, each of the one bit DACs 120, 122, 124 and 126 is clocked at a different time period by the multi phase clocks to provide the corresponding output signal. Moreover, Panasik fails to teach that

the output signal is provided at an output sample rate that is different from the input sample rate as recited in claim 1. Reconsideration of claim 11 is respectfully requested.

Claim 12 depends from claim 11 and further recites an antenna that is operative to propagate a wireless signal at a transmission frequency based on the corresponding analog signal. Since claim 12 depends from claim 11 it is allowable for at least substantially the same reasons as claim 11.

For the reasons described above, claims 1-3, 6-7 and 11-12 are patentable over the Panasik. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Rejection of Claims 20-21 Under 35 U.S.C. §103(a)

Claims 20-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Piesinger as applied to claim 15 above, and further in view of Panasik. Claims 20 and 21 depend from claim 15 which has been amended into allowable form the incorporate the subject matter of claim 22. Accordingly, the rejections of claims 20 and 21 set forth in the office action are now moot.

V. Allowable Subject Matter

Applicant appreciates the indication that Claims 4, 5, 8-10, 13-14, 16-17, 18-19, 22 and 24-26 are allowable, and that claims 27-29 have been allowed.

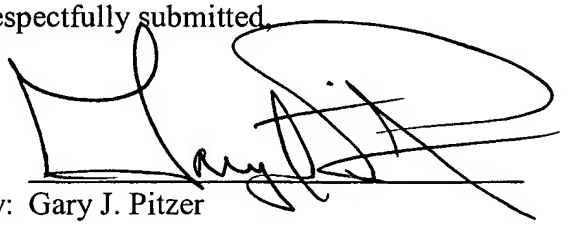
CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

If the Examiner has any questions or if the Applicant or its representative can be of any assistance in connection with prosecution of this application, the Examiner is invited and encouraged to contact the undersigned at the number identified below.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,



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